IN THE SPECIFICATION

1. On page 4 line 18 through page 5, line 5, please amend the text as follows:

--In a third aspect of the invention, an improved data processing apparatus is disclosed. The device generally comprises a processor core, the aforementioned memory interface, at least one macro function, XY memory array, and I/O interface. In one exemplary embodiment, the processor core comprises an extensible ~~RISC-based~~ Reduced Instruction Set Computer (RISC) based digital processor, and the macro function comprises a digital signal processor (DSP). The DSP may be a general purpose DSP, or alternatively any one of a number of algorithmically optimized designs which are adapted to perform certain data processing tasks. The RISC processor and DSP are tightly coupled such that the DSP and memory interface effectively become part of the RISC processor's instruction set, the macro function (DSP) being controlled by, for example, decoded instructions generated by the pipeline decode stage of the RISC processor. Furthermore, peripheral devices can have direct memory access (DMA) capability with respect to the XY memory array via the I/O interface. The components are also advantageously combined into a single-die integrated circuit device. In another embodiment, the device comprises a "3G" ASIC having a plurality of macro blocks including a signal receiver and demodulator, "turbo" or Viterbi decoder, block cyclic redundancy code (CRC) calculation macro, block permute macro, block convolution encoder macro, and modulator and transmitter, all of which are coupled to the core memory array via the memory interface.--